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Performance Analysis of GaN-NW FET under Wide-Range Bias Conditions for Suppressing SCEs: PADRE Simulation Approach

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Abstract: *The continuous scaling of conventional Si-based transistors is increasingly limited by pronounced short channel effects (SCEs), leakage currents, and degraded electrostatic control. In this paper, we present a TCAD simulation of a Gallium Nitride (GaN) Nanowire Field-Effect Transistor (NW-FET) using the MuGFET structure definition tool and the PADRE device simulator, which solves the coupled Poisson and drift-diffusion equations. This proposed device was analyzed under 10 different drain-bias conditions (1–10 V) to investigate the impact of drain-voltage variation with respect to key performance parameters. The evaluated metrics were extracted from linear and logarithmic I–V plots, including a stable V_{th}, SS value of 84-85 mV/dec, drain barrier of 6-19 mV/V, and consistent I_{ON}/I_{OFF} of $\sim 10^7$. These findings provide valuable insights into the design and optimization of next-generation energy-efficient transistors in advanced integrated circuits, particularly for low-power applications.*

Keywords *: GaN nanowire FET; MuGFET; PADRE; TCAD simulation; short-channel effects; DIBL; V_{th} and SS.*

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1.0 Introduction

The continuous scaling of metal–oxide–semiconductor field-effect transistor (MOSFET) technology has been the primary driver of advances in integrated circuits over the past several decades. However, as device dimensions approach the sub-10 nm regime, conventional planar MOSFETs increasingly

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suffer from severe short-channel effects (SCEs), including threshold voltage roll-off, drain-induced barrier lowering (DIBL), increased leakage current, and degraded subthreshold characteristics, all of which adversely affect device reliability, switching performance, and power efficiency (Ratnesh *et al*., 2021). These limitations have motivated the development of advanced multigate transistor architectures capable of providing superior electrostatic control over the channel region.

Among the emerging nanoscale transistor structures, nanowire-based field-effect transistors (NW-FETs) and Gate-All-Around Field-Effect Transistors (GAAFETs) have attracted considerable attention because of their ability to suppress short-channel effects through complete gate enclosure of the channel (Colinge *et al*., 2011; Larrieu *et al*., 2017). The multigate nanowire architecture has been recognized as one of the most effective device configurations for enhancing gate controllability and maintaining device performance under aggressive scaling conditions (Colinge *et al*., 2011). Furthermore, one-dimensional (1D) semiconductor nanostructures, such as nanowires and nanotubes, possess unique electrical, optical, and chemical properties that make them attractive building blocks for next-generation nanoelectronic and optoelectronic devices (Suo *et al*., 2014).

To overcome the limitations of conventional MOSFETs, several advanced transistor architectures have been proposed, including FinFETs, nanosheet FETs, tunnel FETs, and GAAFETs (Mohan *et al*., 2017; Narula & Pandey, 2022). Among these technologies, GAAFETs provide the highest level of electrostatic control because the gate completely surrounds the channel, thereby minimizing leakage current and improving switching behavior (Das *et al*., 2024; Vashishtha & Clark, 2021). Consequently, GAAFETs have emerged as strong candidates for future technology nodes beyond FinFET architectures.

In addition to device geometry, channel material selection plays a critical role in determining transistor performance. Silicon has traditionally dominated semiconductor device fabrication due to its favorable electronic properties and mature manufacturing processes (Rai *et al*., 2024). Nevertheless, wide-bandgap semiconductors such as Gallium Nitride (GaN) are increasingly being investigated because of their superior electron mobility, high critical electric field, excellent thermal conductivity, and remarkable breakdown strength (Suo *et al*., 2014). These characteristics make GaN particularly suitable for high-frequency, high-power, and high-temperature applications where conventional silicon devices may exhibit performance limitations.

Recent studies have demonstrated the significant potential of GaN-based nanowire transistors. For instance, Singh *et al*. (2025) reported that high-k wrapped GaN GAAFETs exhibited enhanced electrostatic control and superior high-frequency performance suitable for Internet of Things (IoT) applications. Similarly, Li *et al*. (2016) demonstrated that GaN nanowire metal–insulator–semiconductor field-effect transistors (MISFETs) achieved a subthreshold swing of approximately 90 mV/dec while maintaining low-power operation. Furthermore, experimental investigations of GaN nanowire devices have revealed excellent thermal stability and sustained performance under elevated temperature conditions, making them promising candidates for aerospace, automotive, and harsh-environment electronics (Vodapally *et al*., 2016).

Several researchers have explored the performance advantages of advanced nanowire and GAAFET architectures. Vashishtha and Clark (2021) compared FinFETs and GAAFETs at the 5 nm technology node using Technology Computer-Aided Design (TCAD)

and compact-model simulations and reported improved current drive capability and reduced leakage currents for GAAFET structures. Das *et al*. (2024) reviewed the evolution from FinFETs to Gate-All-Around Multi-Bridge Channel FETs (MBCFETs) and highlighted substantial improvements in subthreshold slope and leakage suppression. Likewise, Yazeer *et al*. (2016) investigated triangular silicon nanowire transistors using COMSOL Multiphysics and demonstrated enhanced short-channel performance relative to conventional nanowire geometries. Other studies have focused on threshold voltage modeling (Marin *et al*., 2014), low-power gate-all-around structures (Kumar *et al*., 2024), and junctionless nanowire transistor designs (Choi *et al*., 2020), all of which emphasize the importance of geometry and material engineering in nanoscale transistor optimization.

Despite these advances, a significant knowledge gap remains regarding the comprehensive electrical characterization of GaN nanowire GAAFETs under varying drain bias conditions. Most reported studies have concentrated on device performance at fixed operating voltages or have primarily focused on silicon-based GAAFET structures (Das *et al*., 2024; Vashishtha & Clark, 2021). Consequently, limited information exists on how variations in drain voltage influence critical performance parameters such as threshold voltage (V_t), subthreshold swing (SS), drain-induced barrier lowering (DIBL), and ON/OFF current ratio in GaN nanowire GAAFETs. Understanding these relationships is essential for optimizing device design and ensuring reliable operation in future low-power nanoelectronic systems.

Therefore, the aim of this study is to perform a comprehensive TCAD-based investigation of a Gallium Nitride (GaN) nanowire Gate-All-Around Field-Effect Transistor using the MuGFET structure definition platform and the PADRE device simulator. The study systematically evaluates the influence of varying drain bias conditions on key electrical performance metrics, including threshold voltage, subthreshold swing, DIBL, and ON/OFF current ratio.

The significance of this work lies in providing a deeper understanding of the electrostatic behavior and bias-dependent performance of GaN nanowire GAAFETs. The findings are expected to contribute to the optimization of next-generation low-power, high-speed, and thermally robust nanoelectronic devices for applications in advanced integrated circuits, high-frequency electronics, aerospace systems, and emerging semiconductor technologies.

2.0 Device Structure and Simulation

This chapter presents the methodology employed in simulating and analyzing the electrical behavior of Gallium Nitride (GaN) Nanowire Field-Effect Transistors (NW-FETs) using the MuGFET simulation tool, evaluating performance metrics such as V_{th}, SS, DIBL, and ON/OFF current ratio across various V_d. The methodology includes selecting simulation parameters, designing the device structure, specifying biasing conditions, and using techniques to extract key performance metrics.

2.1 Simulation Tool

A robust electronic device simulation platform is essential for understanding the underlying physics governing nanoscale transistor structures and for accurately predicting device behavior before fabrication (Choi *et al*., 2020). In this study, the MuGFET simulation tool was selected because of its capability to model multigate transistor architectures with high accuracy and computational efficiency. Developed at Purdue University, the MuGFET platform provides a flexible environment for defining nanowire geometry, channel dimensions, doping concentrations, mesh structures, and gate configurations required for nanoscale device simulations (Kim *et al*., 2023).

The MuGFET framework incorporates either the PADRE or PROPHET device simulators, both of which were originally developed at Bell Laboratories to facilitate advanced semiconductor device analysis (Hashim, 2024). The PROPHET simulator functions as a partial differential equation solver capable of handling one-, two-, and three-dimensional semiconductor device problems, while PADRE employs a self-consistent solution of the Poisson and drift–diffusion transport equations to generate the electrical characteristics of field-effect transistors (Kim *et al*., 2023). These simulation engines provide detailed information on carrier transport, electrostatic potential distribution, charge density, and current conduction mechanisms, thereby enabling a comprehensive understanding of transistor operation.

The integration of MuGFET with PADRE and PROPH*Et al*lows the generation of essential transistor characteristics, including transfer and output curves, which are valuable for evaluating device performance and investigating the physical mechanisms governing nanowire field-effect transistors (Kim *et al*., 2023). Since both simulators operate within a self-consistent Technology Computer-Aided Design (TCAD) environment, they provide reliable predictions of device behavior under different biasing conditions and structural configurations.

The electrostatic behavior of the GaN nanowire Gate-All-Around Field-Effect Transistor (GAAFET) is governed by the Poisson equation, which describes the relationship between the electric potential and charge distribution within the semiconductor device (Kim *et al*., 2023). The Poisson equation is expressed in Equation (1):

$$\nabla \cdot (\varepsilon \nabla \mathrm{V}) = q(n - p + N_A - N_D) \quad (1)$$

Where ε is the dielectric constant, V the potential, n/p electron/hole density, $N_A \, and \, N_D$ represent ionized donor and acceptor densities respectively, while q the elementary charge, this equation ensures that the electrostatic potential across the nanowire channel reflects the combined influence of external gate bias, channel doping, and charge carriers, which is critical in evaluating gate control and short channel effects of GAAFETs devices (Rewatkar & Joshi, 2017; Kim *et al*., 2023)..

Carrier transport within the device is described using the drift–diffusion transport model, which is widely employed in TCAD simulations of nanoscale semiconductor devices because of its balance between computational efficiency and physical accuracy (Kim *et al*., 2023). In this model, the total current density is expressed as the sum of the drift component arising from the electric field and the diffusion component resulting from carrier concentration gradients. The electron and hole current density equations are given in Equations (2) and (3), respectively:,

$$\vec{J}_n = qn\mu_n\vec{E} + qD_n\nabla n \quad (2)$$

$$\vec{J}_p = qp\mu_P\vec{E} - qD_p\nabla p \quad (3)$$

where $\vec{J}_n$,$\vec{J}_p$ are electron and hole current densities, n, p are carrier concentrations, μ_n,μ_P are mobilities, D_p are diffusion coefficients, and $\vec{E}$ is the electric field. he drift component represents carrier transport under the influence of the electric field generated by the applied gate and drain biases, whereas the diffusion component accounts for carrier movement resulting from concentration gradients within the semiconductor material (Kim *et al*., 2023). The highlighted mechanisms govern the flow of charge carriers through the nanowire channel and significantly influence the electrical characteristics of the device.

The conservation of charge carriers within the transistor is described by the continuity equations for electrons and holes, which relate the temporal variation of carrier concentration to the net current flow and carrier generation–recombination processes. The electron and hole continuity equations are expressed in Equations (4) and (5), respectively:

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla \cdot J_n + G(n,p) - P(n,p) \quad (4)$$

$$\frac{\partial p}{\partial t} = \frac{1}{q}\nabla \cdot J_p + G(n,p) - P(n,p) \quad (5)$$

where G and R represent generation and recombination rates, and $J_{n/p}$ represent electron/hole current density (Kim *et al*., 2023).

2.2 Device Structure Parameters

The three-dimensional (3D) structure of the proposed Gallium Nitride Nanowire Field-Effect Transistor (GaN-NWFET) is illustrated in Fig. 1. In this device, Gallium Nitride (GaN) serves as the channel material extending from the source to the drain region owing to its wide bandgap, high electron mobility, superior thermal stability, and excellent breakdown characteristics, which make it highly suitable for nanoscale and high-performance electronic applications (Suo *et al*., 2014; Singh *et al*., 2025). The channel is completely surrounded by a silicon dioxide (SiO_2) gate dielectric with a dielectric constant ((ε_{ox})) of 3.9 and a thickness of 0,7 nm, thereby enabling enhanced electrostatic control of the channel and effective suppression of short-channel effects.

Table 1: Device parameters for GaN-based GAAFET simulation

Parameter	Symbol	Value	Unit
Gate length	L_g	40	Nm
Diameter	D	10	Nm
Drain voltage	V_d	$1-10$	V
Source/Drain length	L_{SD}	20	nm
Gate voltage	V_g	1	V
Gate work function	Φm	4.5	Ev
S/D doping	N_{SD}	1×10^{20}	cm^{-3}
Channel doping	N_{CH}	1×10^{15}	cm^{-3}
Electron mobility	μn	1000	cm^2/Vs
Relative permittivity	εr	9.0	1
Bandgap	Eg	3.4	eV

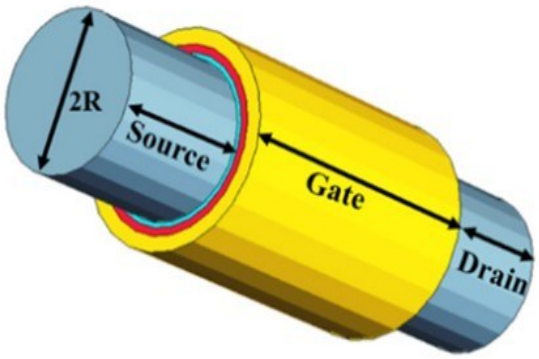

Fig. 1: GaN-Based GAAFET device

The geometrical and material parameters of the proposed device were carefully selected based on established literature and previously reported GAAFET and nanowire transistor designs to achieve optimum electrical performance (Kumar *et al*., 2024; Vashishtha & Clark, 2021). The key structural dimensions and simulation parameters employed in this study are summarized in Table 1. Fig. 1 further presents the complete three-dimensional representation of the proposed GaN-NWFET structure, highlighting the source, drain, gate, dielectric, and nanowire channel regions. Device simulations were performed using the PADRE simulator within the MuGFET TCAD environment, which provides self-consistent solutions of the Poisson, continuity, and drift–diffusion equations for accurate prediction of nanoscale transistor behavior (Kim *et al*., 2023).

3.0 Results and Discussion

Fig.s 2 & 3 illustrate the graphical representation of the transfer characteristics $(I_d - V_g)$ in linear and logarithmic scale for the 40 nm gate length for GaN-based NW-FET, where the V_g is varied from 0.0 nm to 1.0 nm. Also, to be noted that the FET devices were wrapped with SiO_2 dielectric material to submerge the fringing field effects. As shown in Fig, 2, a noticeable increase in the drain current ((I_D)) was observed with increasing gate voltage ((V_{GS})), indicating efficient channel formation and strong electrostatic control of the gate over the conduction channel. The monotonic increase in (I_D) demonstrates the ability of the gate-all-around nanowire structure to effectively modulate carrier concentration within the channel, thereby enhancing device switching performance (Kumar *et al*., 2024; Vashishtha & Clark, 2021).

Furthermore, as the drain voltage ((V_{DS})) increased, a significant enhancement in the ON-state current was observed. This behavior can be attributed to the increase in the lateral electric field along the channel, which promotes more efficient carrier transport from the source to the drain region. The enhanced carrier mobility and improved charge transport characteristics contribute to higher current drive capability and better device performance. The transfer characteristics also exhibit a smooth transition from the OFF-state to the ON-state, reflecting excellent gate controllability and stable switching behavior, which are essential requirements for low-power and high-performance nanoelectronic applications (Kumar *et al*., 2024; Das *et al*., 2024).

The observed behavior further confirms the effectiveness of the GaN nanowire Gate-All-Around Field-Effect Transistor (GAAFET) architecture in suppressing short-channel effects while maintaining strong electrostatic integrity. Such characteristics are desirable for future nanoscale integrated circuits where high ON-state current, low leakage current, and reliable switching operation are critical performance metrics (Colinge *et al*., 2011; Singh *et al*., 2025).

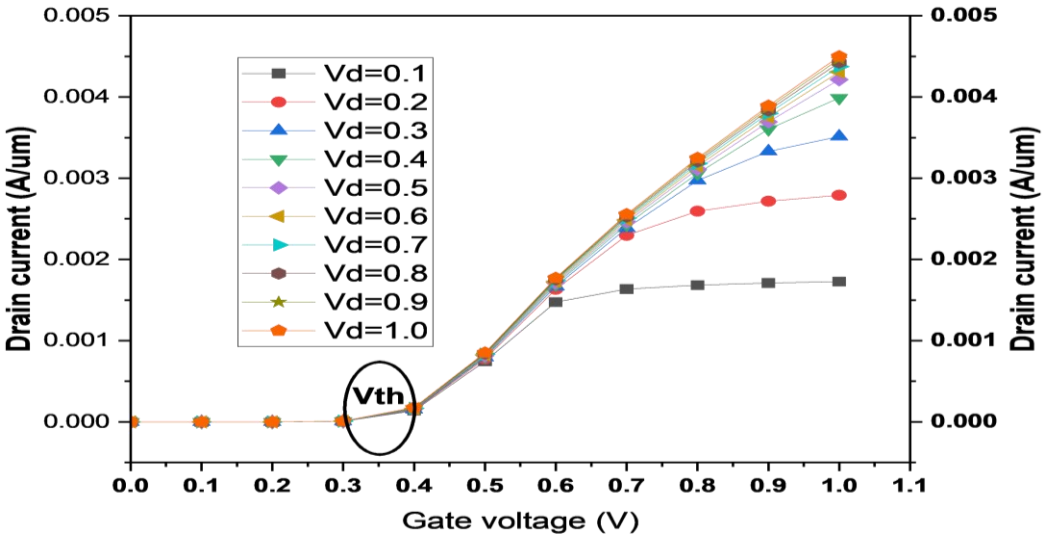

Fig. 2: I_d - V_g characteristics of GaN GAAFET in Linear Scale

While Fig. 3 shows the transfer characteristics in logarithmic scale, which provides insight into the subthreshold region, leakage behavior demonstrating a steep transition between OFF-state and ON-state, giving insight in to switching efficiency, a leakage current is observed at low gate voltages, which are essential for low-power applications. As the

drain voltage ((V_{DS})) increases, a slight shift of the transfer characteristics toward lower gate voltage ((V_{GS})) is observed, indicating a gradual reduction in the threshold voltage ((V_T)). This behavior is attributed to the drain-induced barrier lowering (DIBL) effect, a common short-channel phenomenon in nanoscale transistors whereby the electric field originating from the drain extends into the channel region and partially reduces the source-to-channel potential barrier (National Engineering College *et al*., 2016; Kumar *et al*., 2024).

The reduction in the potential barrier facilitates carrier injection from the source into the channel at lower gate voltages, resulting in an apparent decrease in threshold voltage as (V_{DS}) increases. Although the observed shift confirms the presence of DIBL, its relatively small magnitude suggests that the proposed GaN nanowire Gate-All-Around Field-Effect Transistor (GAAFET) maintains strong electrostatic control over the channel. This behavior highlights the effectiveness of the gate-all-around architecture in suppressing short-channel effects and preserving device stability under varying bias conditions (Colinge *et al*., 2011; Vashishtha & Clark, 2021). Consequently, the device demonstrates excellent scalability and suitability for low-power, high-performance nanoelectronic applications.

These I_d - V_g characteristics enable accurate extraction of SS, DIBL, and I_{on}/I_{off} ratio, which are critical for evaluating short-channel effects and low-power performance.

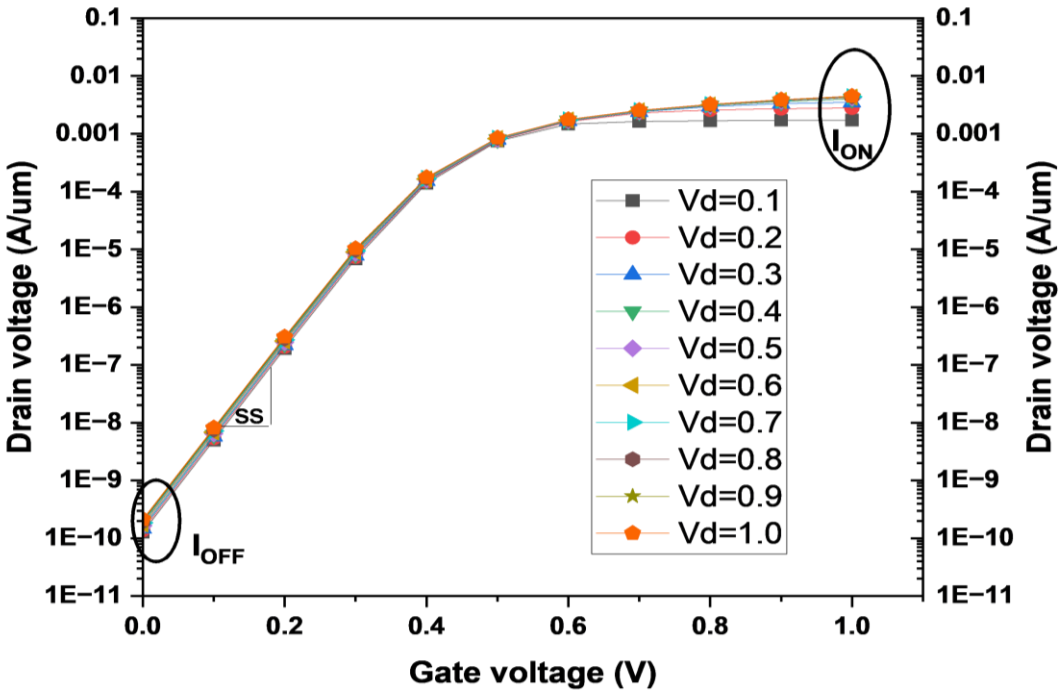

Fig. 3: $I_d - V_g$ characteristics of GaN GAAFET in Logarithm

3.1 Current Ratio ($\frac{I_{ON}}{I_{OFF}}$) vs Drain Voltage

The determination of current ratio by extracting the minimum and maximum current from the drain current (I_d) vs gate voltage (V_g) sweep for individual drain voltages (V_d). Fig. 4 illustrates how drain voltage (V_d) impacts the current ratio (I_{on}/I_{off}) the maximum value of I_{on}/I_{off} occurs at $V_d = 1.0\,V$ and subsequently drops to $1.36 \times 10^7\,A/\mu m$ at V_d $0.1\,V$, as shown in Fig. 4. This occurs due to the strong and symmetrical electrostatic gate control over the channel, which also improved

the I_{on}/I_{off} ratio of the device [20]. It can be noticed that it maintains a high current ratio on the order of $10^7\ A/\mu m$ across the V_d biasing conditions, primarily owing to wide bandgap of channel material and GAA structure, which suppresses leakage current and ensures strong electrostatic control, respectively indicating excellent switching performance of the device [5], [12]. As the drain voltage increases, the current ratio shows a slight variation, which can be attributed to the combined effect of increasing ON-current and a marginal increase in OFF-state leakage, this trend is consistent with the results obtained by Yazeer *et al.* (2016) on triangular gate GAAFE. The consistently high ratio across the entire bias range demonstrates the potential of GaN-based GAAFETs for low-power electronic applications, while the large ON-state drive current enables fast switching speed backed by the results obtained by Ratnesh *et al.* (2021). These findings highlight the current ratio behavior of this proposed device at various drain voltages.

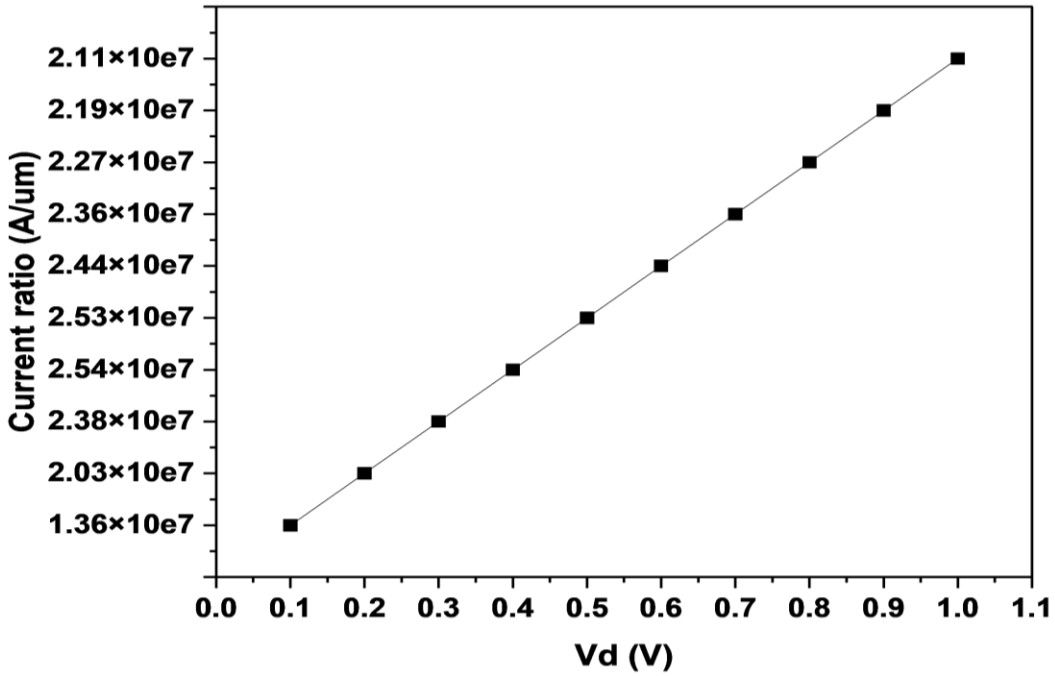

Fig. 4: Variation of I_{ON}, $I_{OFF,}$ and Current Ratio of GaN-Based GAAFET with Drain Voltage

3.2 Impact of Drain Voltage (V_d) on Threshold Voltage (V_{th})

The variation of V_{th} as a function of V_d is presented in Fig. 5, from the described figure., a clear decreasing trend in threshold voltage is observed as V_d increases, this trend indicating the presence of barrier lowering, a characteristic of short channel effect in nanoscale transistors. At $V_d = 0.1\,V$, the device exhibits a threshold voltage of 0.3891 V, which gradually decreases to $0.3799\ V$ at $V_d = 1.0\,V$, amounting to a total shift of approximately 9.2 mV. The most significant drop occurs in the low drain bias regime $(0.1 - 0.3\,V)$, where V_{th} decreases from $0.3891\ V$ to $0.3858\ V$ (a reduction of $\sim 3.3\ mV$). This behavior indicates the partial penetration of the drain electric field into the channel region, particularly at low gate bias conditions, where the drain potential begins to influence the channel electrostatics. As a result, the source-to-channel energy barrier is reduced, leading to a weakening of the effective gate control over the channel charge distribution. Such behavior is characteristic of nanoscale transistors and is

commonly associated with drain-induced barrier lowering (DIBL), where the drain field competes with the gate field in controlling carrier transport (Marin *et al*., 2014). Nevertheless, the relatively small shift observed in the transfer characteristics suggests that the proposed GaN nanowire Gate-All-Around Field-Effect Transistor maintains strong electrostatic integrity, thereby mitigating the adverse effects of short-channel phenomena and ensuring stable device operation across the investigated bias range (Colinge *et al*., 2011; Vashishtha & Clark, 2021).

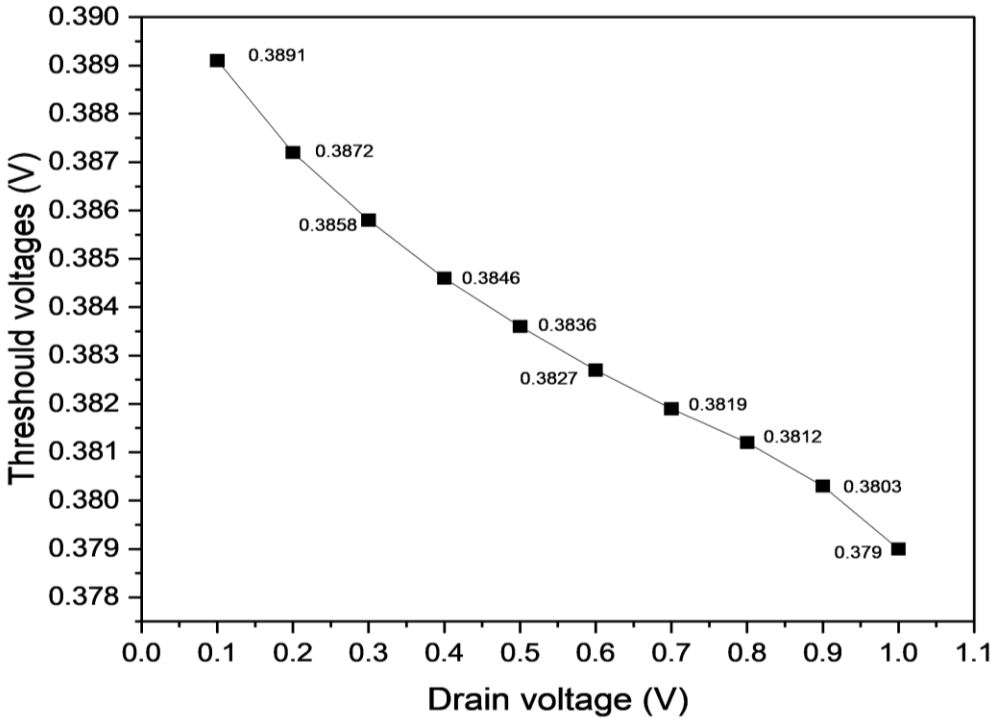

Fig. 5: Threshold voltage behaviour of GaN-based GAAFET from MuGFET

Beyond $V_d = 0.4\,V$, the reduction in V_{th} becomes more gradual and eventually tends toward saturation. For instance, between $0.7\,V$ and $1.0\,V$, the total shift is only about $2\,mV$, suggesting that the device retains strong electrostatic integrity at higher drain biases. This stability is attributed to the superior gate coupling provided by GAA geometry, which effectively suppresses short-channel effects compared to other device architectures. Overall, the observed V_{th} roll-off of only $\sim 9.2\,mV$ across the $0.1-1.0\,V$ range

3.3 Impact of Drain Voltage (V_d) on Drain Induced Barrier lowering (DIBL) and Subthreshold Swing (SS)

When a drain voltage ((V_{DS})) is applied, the electric field originating from the drain region extends into the channel and influences the potential barrier at the source–channel junction. As the drain voltage increases, the source-to-channel energy barrier is lowered, thereby facilitating carrier injection from the source into the channel even at lower gate voltages. This phenomenon is known as Drain-Induced Barrier Lowering (DIBL) and is one of the most significant short-channel effects (SCEs) encountered in nanoscale transistors. DIBL reduces the effectiveness of gate control over the channel, resulting in a decrease in threshold voltage and an increase in off-state leakage current (Kumar *et al*., 2024; Marin *et al*., 2014).

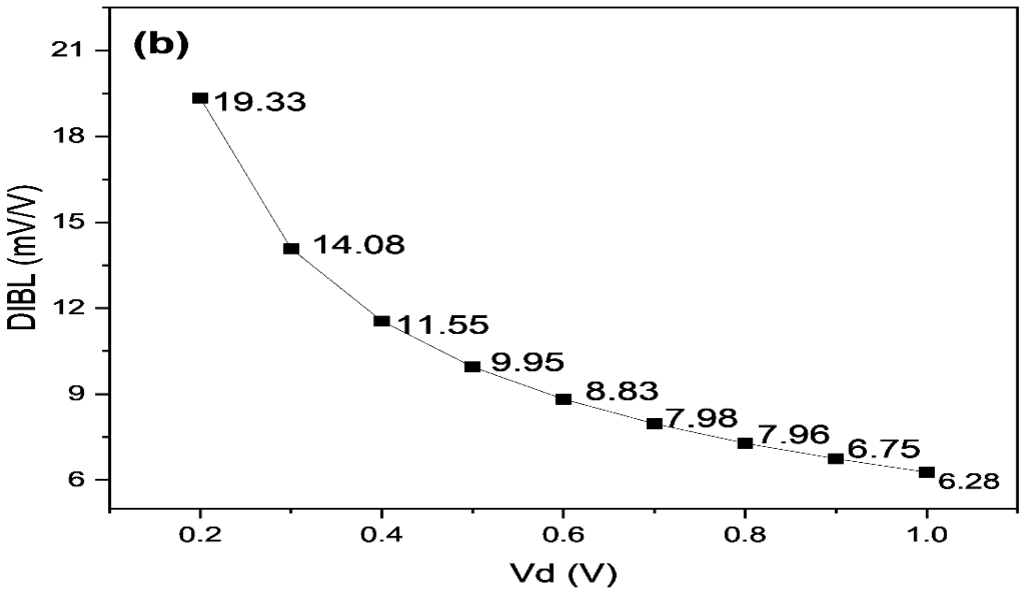

Fig. 6: DIBL behavior of GaN-based GAAFET

DIBL is widely used as a measure of the electrostatic integrity of a transistor, with lower DIBL values indicating stronger gate control and better suppression of short-channel effects. The DIBL parameter can be expressed as (Kumar *et al*., 2024):

$$DIBL = \frac{\Delta Vth}{\Delta Vd} \quad (6)$$

Fig. 6 represents the extracted DIBL values as a function of drain voltage. The DIBL values exhibit a clear decreasing trend with increasing drain bias. At $V_d = 0.2$ V, the device exhibits a maximum DIBL of $19.33\ mV/V$, which progressively decreases to $6.28\ mV/V$ at $V_d = 1.0$ V. This decline indicates that the influence of the drain potential on the channel barrier is strongest at low drain voltages but becomes less pronounced as V_d increases which is in agreement with the result obtained by Kumar *et al.,* (2024) which clearly illustrates the reduction in DIBL highlights the excellent electrostatic control of the gate all around geometry, this effectively mitigates short channel effects even under higher drain biases.

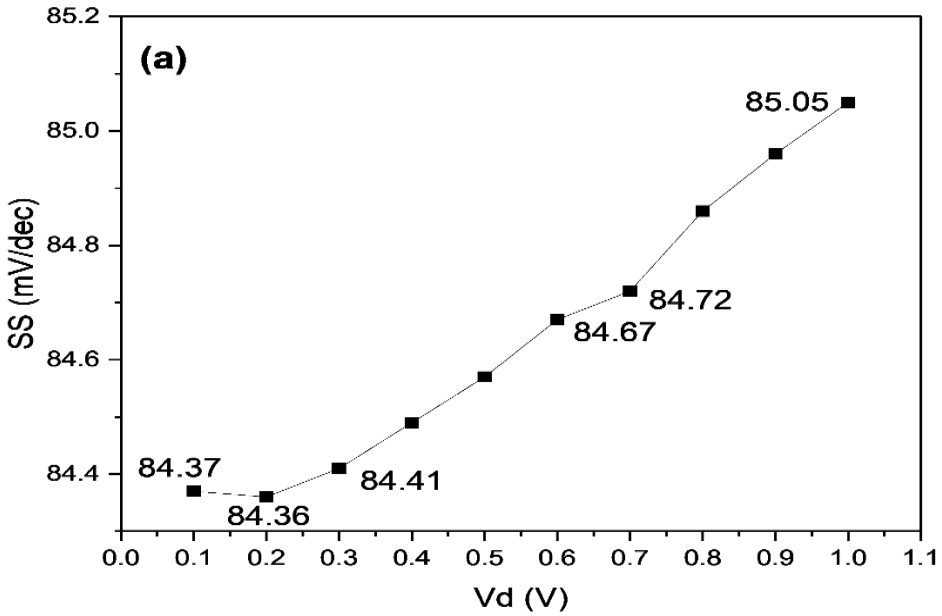

Fig. 7*: SS Behavior of GaN-based GAAFET*

In contrast, the subthreshold swing (SS) remains remarkably stable across the range of drain bias examined. It changes slightly, from $84.37\ mV/dec$ to $85.05\ mV/dec$ at $V_d = 0.1\ V\ and\ 1.0\ V$ respectively, with a fluctuation of less than $1\ mV/dec$. The observed stability indicates that the subthreshold characteristics of the device are largely insensitive to variations in drain bias. The subthreshold swing (SS) remains nearly constant across the investigated drain voltage range, demonstrating excellent gate electrostatic control over the channel region. Although the extracted SS values are slightly higher than the theoretical thermionic limit of 60 mV/dec at room temperature (300 K), they remain within the range reported for high-performance nanoscale GaN-based transistors and gate-all-around device architectures (Hashim, 2024; Mohan *et al*., 2017). This behavior suggests efficient gate-to-channel coupling and effective modulation of the channel potential, which are essential for achieving reliable switching characteristics and minimizing power dissipation in low-power electronic circuits.

Furthermore, the minimal variation in SS with increasing drain voltage indicates that the drain electric field exerts only a limited influence on the subthreshold conduction mechanism. This reflects the strong electrostatic integrity of the proposed GaN nanowire Gate-All-Around Field-Effect Transistor (GAAFET), where the surrounding gate structure effectively screens the channel from drain-induced perturbations. Consequently, the device exhibits stable switching behavior and enhanced operational reliability under different biasing conditions (Mohan *et al*., 2017; Vashishtha & Clark, 2021).

The combination of low DIBL values and nearly constant subthreshold swing provides strong evidence that the proposed device architecture effectively suppresses short-channel effects. Such performance characteristics are highly desirable for aggressively scaled transistor technologies, where maintaining threshold voltage stability and minimizing leakage currents are critical design requirements. Therefore, the simulated GaN nanowire GAAFET demonstrates significant potential for application in next-generation low-power, high-speed, and energy-efficient nanoelectronic systems, where superior electrostatic control and robust

switching performance are required (Narula & Pandey, 2022; Das *et al*., 2024).

4.4 Comparison with Existing Literatures

To evaluate the performance matrices of the proposed GaN nanowire GAAFET, a comparison with previously reported findings on Si and GaN-based devices is presented in Table 2 at drain voltage of 0.6 V demonstrating good performance with notable distinctions in both channel materials.

Table 1: Comparison Table with Other Results

Channel material	Lg (nm)	I_{ON} $(A/\mu m)$	I_{OFF} $(A/\mu m)$	I_{ON}/I_{OFF} $(A/\mu m)$	SS (mV/dec)	DIBL (mV/V)	References
Si	40	1.4×10^{-4}	10^{-9}	1.1×10^{5}	59	-100	[18]
Ga N	300	–	2.0×10^{-11}	10^{8}	265	–	[12]
GaN	–	7.3×10^{-5}	–	$> 10^{5}$	15	–	[23]
GaN	–	10.2×10^{-6}	9.8×10^{-12}	1.04×10^{6}	65.37	32.6	[24]
Si	300	3.74×10^{-5}	6×10^{-17}	10^{12}	60	12.22	[11]
GaN	40	4.31×10^{-3}	1.76×10^{-10}	2.44×10^{7}	84.67	8.83	Proposed study

4.0 Conclusion

A comprehensive TCAD-based simulation study of Gallium Nitride (GaN) Nanowire Gate-All-Around Field-Effect Transistors (GaN NW-FETs) was conducted using the MuGFET structure definition tool and the PADRE device simulator under varying drain bias conditions. The investigation revealed that drain voltage significantly influences key electrical performance parameters, including threshold voltage ((V_T)), subthreshold swing (SS), drain-induced barrier lowering (DIBL), and the ON/OFF current ratio. As the drain bias increased, a slight reduction in threshold voltage and a corresponding increase in DIBL were observed, reflecting the influence of the drain electric field on channel electrostatics. However, the relatively low DIBL values obtained indicate that the proposed device maintains strong gate control and effective suppression of short-channel effects.

The transfer characteristics demonstrated a smooth transition between the OFF-state and ON-state, while the high ON/OFF current ratio confirmed excellent switching capability and low leakage current operation. In addition, the nearly constant subthreshold swing across the investigated drain bias range indicates robust gate-to-channel coupling and stable subthreshold behavior. These findings collectively demonstrate that the gate-all-around nanowire architecture provides superior electrostatic integrity, enabling reliable operation even under varying bias conditions.

The present study establish the proposed GaN nanowire transistor as a promising candidate for next-generation low-power, high-speed, and energy-efficient nanoelectronic applications. The combination of strong electrostatic control, high current drive capability, low leakage current, and reduced susceptibility to short-channel effects highlights the suitability of GaN nanowire GAAFETs for future nanoscale integrated circuits and advanced semiconductor technologies.

Based on the findings of this study, the following recommendations are proposed for future research:

(i) Experimental validation of the simulated GaN nanowire GAAFET structures should be undertaken to verify the simulation results and establish the practical feasibility of device fabrication.

(ii) The investigation of alternative high-k gate dielectric materials such as HfO_2, ZrO_2, and Al_3O_2 is recommended to further enhance gate capacitance, reduce leakage current, and improve electrostatic control at ultra-scaled dimensions.

(iii) Future studies should explore the impact of channel geometry optimization, including variations in nanowire diameter, gate length, and oxide thickness, on device performance and short-channel-effect suppression.

(iv) Comparative simulation analyses involving emerging semiconductor materials, such as carbon nanotubes (CNTs), silicon–germanium (SiGe), indium gallium arsenide (InGaAs), molybdenum disulfide (MoS_2), and graphene, are recommended to identify the most suitable channel materials for sub-5 nm technology nodes.

(v) Further investigations incorporating temperature-dependent and reliability analyses are necessary to evaluate the long-term performance of GaN nanowire GAAFETs in high-frequency, high-power, and harsh-environment applications.

These future research directions will contribute to the continued development and optimization of nanowire transistor technologies for advanced nanoelectronic and integrated circuit applications.

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Declarations

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Author Contributions
A. B. S. conceived and designed the study, developed the GaN-NW FET model, conducted the PADRE/TCAD simulations, analyzed the device performance parameters, and prepared the manuscript. I. M. M., M. S., S. S. A., and A. A. S. contributed to simulation procedures, data analysis, interpretation of results, and manuscript review. A. A. B., I. S., and H. I. contributed to validation, technical interpretation, critical revision, and final approval of the manuscript.